Intel® E7221 Chipset Memory Controller Hub (MCH)

White Paper

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Contents

Figures

Revision History

Revision Number	Description	Revision Date
-001	Initial Release.	October 2004

1 Introduction

This document details the Intel® E7221 chipset memory controller hub (MCH) key benefits and operation. It is intended for a technical audience interested in learning about the E7221 chipset architecture.

Please refer to *the Intel® I/O Controller Hub 6 / 6R / 6W (ICH6) / (ICH6R) / (ICH6W) White Paper* for complete details on the I/O hub controller.

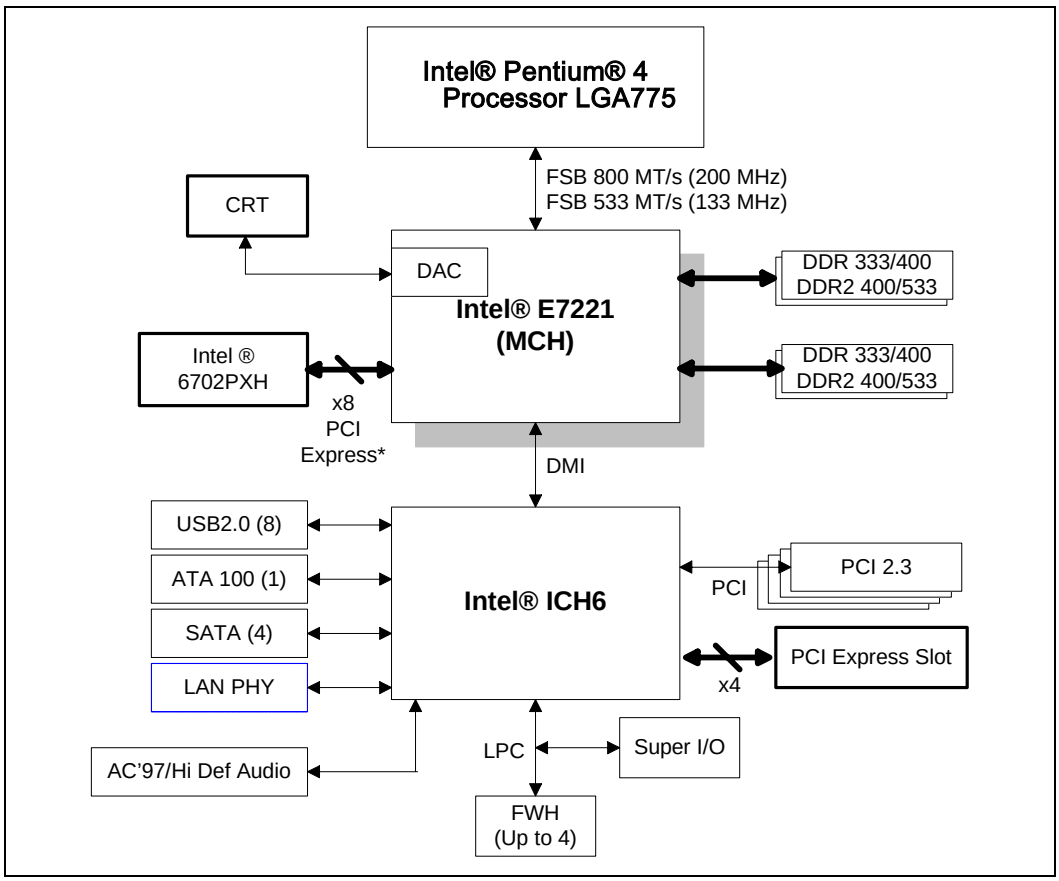
For great server application flexibility, the Intel® E7221 chipset is specifically designed to support Intel® Extended Memory 64 Technology* (Intel® EM64T) enabling 64-bit memory addressability. Select versions of the Pentium 4 processor support Intel® Extended Memory 64 Technology* (Intel® EM64T) as an enhancement to Intel's IA-32 architecture on server platforms. This enhancement enables the processor to execute operating systems and applications written to take advantage of Intel® EM64T. Further details on the 64-bit extension architecture and programming model can be found in the Intel® Extended Memory 64 Technology Software Developer Guide at http://developer.intel.tom/technology/64bitextensions/.

*Intel® Extended Memory 64 Technology (Intel® EM64T) requires a computer system with a processor, chipset, BIOS, OS, device drivers and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending upon your hardware and software configurations. Intel EM64T-enabled OS, BIOS, device drivers and applications may not be available. Check with your vendor for more information.

The E7221 chipset supports PCI Express* and DDR/DDR2 Chipset for the Intel® Pentium® 4 processor in the LGA775 package. The E7221 chipset, with its enhanced architecture, delivers an efficient high-bandwidth communication channel connecting the processor, system memory, I/O subsystem, and other components together to deliver a stable high performance desktop or server platform solution. The E7221 chipset also provides an integrated graphics port.

Figure 1 illustrates how the E7221 chipset connects the processor and various components to make up a complete E7221-based server platform.

Figure 1. Intel® E7221 Chipset Block Diagram



The introduction of the E7221 chipset brings high performance, flexibility and stability to Pentium 4 processor-based systems. With the support of 533 MT/s and 800 MT/s processor system bus, single- or dual-channel DDR 333/400 or DDR2 400/533 system memory, discrete cards, the E7221 chipset provides high system flexibility and scalability. In addition, the E7221 Chipset-based platforms use a single, innovative Intel® software stack, adding stability to the whole platform.

1.1 Processor Interface

The E7221 chipset supports the host bus frequencies of 533 MT/s and 800 MT/s. By providing a bandwidth of up to 6.4 GB/s with 800 MT/s-enabled processors, the E7221 chipset delivers higher throughput when accessing memory and I/O devices, to improve system performance. The 32-bit host addressing is supported, and up to 4 GB of the processor's memory address space is decoded. The E7221 chipset implements its own cache line size of 64 bytes to match the cache line size of the processor. This allows an entire 64-byte cache line to be transferred in two bus clocks, enabling faster data transfers for today's demanding applications. It also supports Dynamic Bus Inversion (DBI), which limits the number of data signals that are driven low on the bus on each data phase. This performance significantly decreases the power consumption of the E7221 chipset. In addition, the E7221 chipset host bus implements GTL+ on die termination to help reduce the system BOM cost.

1.2 System Memory Interface

The E7221 chipset memory interface is designed to be flexible and can be configured through a set of registers to support either single- or dual-channels of DDR (333 MHz or 400 MHz DDR) or DDR2 memory (400 MHz or 533 MHz DDR2) SDRAM memory. This allows up to 8.5 MB/s of memory bandwidth available, providing a balanced platform. DDR2 memory capability supports two data operations being completed within one clock cycle, resulting in faster data transfer and higher memory bandwidth. This translates into twice the throughput of regular SDRAM. The E7221 chipset memory interface can support up to four double-sided DIMMs for a maximum of 4 GB of system memory. The memory technologies supported are 256-Mb, 512-Mb, and 1-Gb SDRAM technologies.

The E7221 chipset is equipped with many advanced system memory interface features to create a balanced performance environment for the platform. Twelve pairs of DDR2 system memory clocks are integrated into the MCH. This eliminates the need for external memory clocks to the DIMMs, and allows better control of system timings for higher system robustness. The memory controller supports the memory thermal management capability that increases the system reliability by decreasing thermal stress on the system memory and the E7221 chipset.

With two 64-bit wide data channels, the memory controller supports up to 64 simultaneously open pages (four ranks of eight bank devices * 2 channels) in dual-channel mode and up to 32 open pages in single-channel mode, reducing the access time to system memory. The MCH also supports Data Masking by providing eight additional data masking signals from the MCH to memory. Byte writes of less than a Qword are allowed to increase memory bandwidth.

New to the E7221 chipset is support of interleaved mode. This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels, and the switch happens after each cache line (64-byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. To achieve interleaved mode, both channels of memory must be populated with equal memory capacity, but the technology and device width may vary from one channel to the other.

1.3 Direct Media Interface

The E7221 chipset utilizes the Direct Media Interface (DMI) as the chip-to-chip connection between the MCH and the I/O controller hub 6 (Intel® ICH6). This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

1.4 Integrated Graphics Interface

The E7221 chipset includes an integrated graphics engine that supports standard SVGA drivers with analog display capabilities.

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2 Summary

The E7221 chipset enables ultimate flexibility with different system bus speeds, memory configurations, and graphics solutions. The E7221 chipset supports 800 MT/s and 533 MT/s system bus for LGA775 processors, 333 MHz/400 MHz DDR and 400 MHz/533 MHz DDR2 memory in single- or dual-channel mode, and integrated graphics. Intel E7221 Chipset-based platforms also offer integrated Hi-Speed USB 2.0, High Definition Audio for improved sound quality and new audio usage models and enhanced RAID support. The E7221 chipset ensures that tomorrow's applications will run best on Pentium 4 processor platforms.

The E7221 chipset enables lower system price points with graphics and hi-speed USB 2.0 integration. The E7221 chipset delivers a complete range of support for the Pentium® 4 processor. This chipset is a great choice for users who want superb graphics quality for the latest digital entertainment. It is also an ideal solution for business users who demand highly stable drivers.

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